IN THE CLAIMS:

1. (Original) A double-edge-trigger flip-flop comprising:

a first pass gate controlled by a clock signal and an inverted signal of the clock for passing an input;

a second pass gate controlled by the clock signal and the inverted signal of the clock for passing the input in a complementary manner with regard to the first pass gate;

a first signal passing module for further passing the input passed by the first pass gate into a third pass gate controlled by the clock signal and the inverted signal of the clock for generating a first part of an output of the flip-flop, wherein the third pass gate passes the input in a complementary manner with regard to the first pass gate; and

a second signal passing module for further passing the input passed by the second pass gate into a fourth pass gate controlled by the clock signal and the inverted signal of the clock for generating a second part of the output, wherein the fourth pass gate passes the input in a complementary manner with regard to the second pass gate.

2. (Original) The flip-flop of claim 1 further comprising a driver module passing the first part of the output on a first edge of the clock input and passing the second part of the output on a second edge of the clock input.

3. (Original) The flip-flop of claim 1 wherein the first signal passing module and the second signal passing module are inverters.

4. (Currently Amended) The flip-flop of claim 1 wherein the first signal passing module and the second signal passing module are NAND gates receiving a flag signal together with the passed input wherein the flag signal disenables the flip-flop when it is asserted.

5. (Original) The flip-flop of claim 1 wherein the first and fourth pass gates have a PMOS and an NMOS transistor connected in parallel for passing the input with the PMOS transistors thereof controlled by the clock input and the NMOS transistors thereof controlled by the inverted signal of the clock input.

6. (Original) The flip-flop of claim 1 wherein the second and third pass gates have a PMOS and an NMOS transistors connected in parallel for passing the input with the NMOS transistors thereof controlled by the clock input and the PMOS transistors thereof controlled by the inverted signal of the clock input.

7. (Original) A double-edge-trigger flip-flop comprising:

a first pass gate passing an input when a clock input having a low value;

a second pass gate passing the input when the clock input having a high value;

a first signal passing module for further passing the input passed by the first pass gate into a third pass gate which passes the input when the clock has a high value to generate a first output;

a second signal passing module for further passing the input passed by the second gate into a fourth pass gate which passes the input when the clock has a low value to generate a second output; and

a driver module passing the first output as an output of the flip-flop on the rising edge of the clock input and passing the second output as the output of the flip-flop on the falling edge of the clock input.

8. (Original) The flip-flop of claim 7 wherein the first signal passing module and the second signal passing module are inverters.

9. (Currently Amended) The flip-flop of claim 7 wherein the first signal passing module and the second signal passing module are NAND gates receiving a flag signal together with the passed input wherein the flag signal disenables the flip-flop when it is asserted.

10. (Original) The flip-flop of claim 7 wherein the first and fourth pass gates have a PMOS and an NMOS transistor connected in parallel for passing the input with the PMOS transistors thereof controlled by the clock input and the NMOS transistors thereof controlled by an inverted signal of the clock input.

11. (Original) The flip-flop of claim 7 wherein the second and third pass gates have a PMOS and an NMOS transistors connected in parallel for passing the input with the NMOS transistors thereof controlled by the clock input and the PMOS transistors thereof controlled by an inverted signal of the clock input.

12. (Original) A double-edge-trigger flip-flop comprising:

a first pass gate controlled by a clock signal and an inverted signal of the clock for passing an input;

a second pass gate controlled by the clock signal and the inverted signal of the clock for passing the input in a complementary manner with regard to the first pass gate;

a first signal passing module for further passing the input passed by the first pass gate into a third pass gate controlled by the clock signal and the inverted signal of the clock for generating a first part of an output of the flip-flop, wherein the third pass gate passes the input in a complementary manner with regard to the first pass gate;

a second signal passing module for further passing the input passed by the second pass gate into a fourth pass gate controlled by the clock signal and the inverted signal of the clock for generating a second part of the output, wherein the fourth pass gate passes the input in a complementary manner with regard to the second pass gate; and

a driver module passing the first part of the output on a first edge of the clock input and passing the second part of the output on a second edge of the clock input,

wherein the first and fourth pass gates have a PMOS and an NMOS transistor connected in parallel for passing the input with the PMOS transistors thereof controlled by the clock input and the NMOS transistors thereof controlled by the inverted signal of the clock input, and

wherein the second and third pass gates have a PMOS and an NMOS transistors connected in parallel for passing the input with the NMOS transistors thereof controlled by the clock input and the PMOS transistors thereof controlled by the inverted signal of the clock input.

13. (Original) The flip-flop of claim 12 wherein the first signal passing module and the second signal passing module are inverters.

14. (Currently Amended) The flip-flop of claim 12 wherein the first signal passing module and the second signal passing module are NAND gates receiving a flag signal together with the passed input.

15. (Original) A method for passing an input through a double-edge-trigger flip-flop, the method comprising:

passing an input through a first pass gate controlled by a clock signal and an inverted signal of the clock;

passing the input through a second pass gate controlled by the clock signal and the inverted signal of the clock in a complementary manner with regard to the first pass gate;

passing the input passed by the first pass gate through a first signal passing module;

passing the input passed by the first signal passing module to a third pass gate controlled by the clock signal and the inverted signal of the clock for generating a first part of an output of the flip-flop, wherein the third pass gate passes the input in a complementary manner with regard to the first pass gate;

passing the input passed by the second pass gate through a second signal passing module;

passing the input passed by the second signal passing module to a fourth pass gate controlled by the clock signal and the inverted signal of the clock for generating a second part of

the output, wherein the fourth pass gate passes the input in a complementary manner with regard to the second pass gate,

wherein the first and second parts of the output are produced upon two edges of the clock signal sequentially.

16. (Original) The method of claim 15 further comprising passing the first and second parts of the output through a driver module.

17. (Original) The method of claim 16 wherein the driver module is an inverter.

18. (Original) The method of claim 15 wherein the first signal passing module and the second signal passing module are inverters.

19. (Currently Amended) The method of claim 15 wherein the first signal passing module and the second signal passing module are NAND gates receiving a flag signal together with the passed input wherein when the flag signal disenables the flip-flop when it is asserted.

20. (Original) The method of claim 15 wherein the first and fourth pass gates have a PMOS and an NMOS transistor connected in parallel for passing the input with the PMOS transistors thereof controlled by the clock input and the NMOS transistors thereof controlled by the inverted signal of the clock input, and wherein the second and third pass gates have a PMOS and an NMOS transistors connected in parallel for passing the input with the NMOS transistors thereof controlled by the clock input and the PMOS transistors thereof controlled by the inverted signal of the clock input.